74AHC1G17; 74AHCT1G17

Single Schmitt trigger buffer

Rev. 1 — 18 March 2014

Product data sheet

1. General description

The 74AHC1G17 and 74AHCT1G17 are single buffers with Schmitt-trigger inputs. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- ESD protection:
    - HBM JESD22-A114E: exceeds 2000 V
    - MM JESD22-A115-A: exceeds 200 V
    - CDM JESD22-C101C: exceeds 1000 V
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- Specified from –40 °C to +125 °C

3. Applications

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G17GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHCT1G17GW				
74AHC1G17GV	–40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74AHCT1G17GV				

Table 1. Ordering information *…continued*

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G17GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AHCT1G17GM				
74AHC1G17GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891
74AHCT1G17GF				

5. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AHC1G17GW	AJ
74AHCT1G17GW	CJ
74AHC1G17GV	A17
74AHCT1G17GV	C17
74AHC1G17GM	AJ
74AHCT1G17GM	CJ
74AHC1G17GF	AJ
74AHCT1G17GF	CJ

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

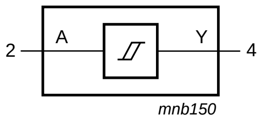


Fig 1. Logic symbol

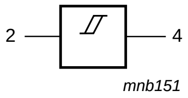


Fig 2. IEC logic symbol

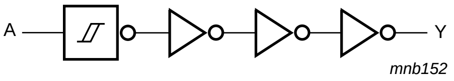


Fig 3. Logic diagram

7. Pinning information

7.1 Pinning

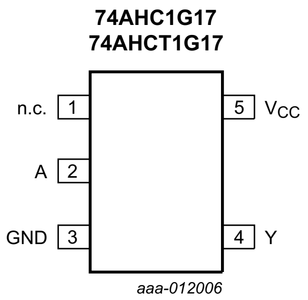
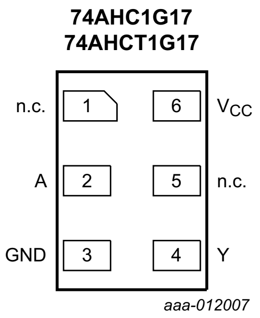
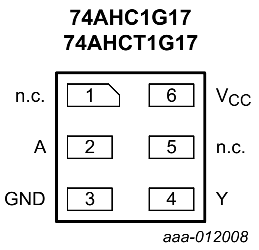


Fig 4. Pin configuration SOT353-1 and SOT753



Transparent top view

Fig 5. Pin configuration SOT886



Transparent top view

Fig 6. Pin configuration SOT891

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT353-1/SOT753	SOT886/SOT891	
n.c.	1	1	not connected
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V_{CC}	5	6	supply voltage

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
A	Y
L	L
H	H

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	–20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		–75	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC1G17			74AHCT1G17			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C

11. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G17										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = -50\ \mu A$; $V_{CC} = 2.0$ V	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50\ \mu A$; $V_{CC} = 3.0$ V	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50\ \mu A$; $V_{CC} = 4.5$ V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.58	-	-	2.48	-	2.40	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = 50\ \mu A$; $V_{CC} = 2.0$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 3.0$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 4.5$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 3.0$ V	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0$ mA; $V_{CC} = 4.5$ V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.0	-	10	-	40	µA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF
74AHCT1G17										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}; $V_{CC} = 4.5$ V								
		$I_O = -50\ \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0$ mA	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}; $V_{CC} = 4.5$ V								
		$I_O = 50\ \mu A$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0$ mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.0	-	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = 3.4$ V; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

11.1 Transfer characteristics

Table 8. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). See Figure 9 and Figure 10.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G17										
V_{T+}	positive-going threshold voltage	V_{CC} = 3.0 V	-	-	2.2	-	2.2	-	2.2	V
		V_{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
		V_{CC} = 5.5 V	-	-	3.85	-	3.85	-	3.85	V
V_{T-}	negative-going threshold voltage	V_{CC} = 3.0 V	0.9	-	-	0.9	-	0.9	-	V
		V_{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
		V_{CC} = 5.5 V	1.65	-	-	1.65	-	1.65	-	V
V_H	hysteresis voltage	V_{CC} = 3.0 V	0.3	-	1.2	0.3	1.2	0.25	1.2	V
		V_{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.35	1.4	V
		V_{CC} = 5.5 V	0.5	-	1.6	0.5	1.6	0.45	1.6	V
74AHCT1G17										
V_{T+}	positive-going threshold voltage	V_{CC} = 4.5 V	-	-	2.0	-	2.0	-	2.0	V
		V_{CC} = 5.5 V	-	-	2.0	-	2.0	-	2.0	V
V_{T-}	negative-going threshold voltage	V_{CC} = 4.5 V	0.5	-	-	0.5	-	0.5	-	V
		V_{CC} = 5.5 V	0.6	-	-	0.6	-	0.6	-	V
V_H	hysteresis voltage	V_{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.35	1.4	V
		V_{CC} = 5.5 V	0.4	-	1.6	0.4	1.6	0.35	1.6	V

12. Dynamic characteristics

Table 9. Dynamic characteristics

GND = 0 V; $t_r = t_f \leq 3.0$ ns. For waveform, see Figure 7. For test circuit, see Figure 8.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G17										
t_{pd}	propagation delay	A to Y; [1]								
		V_{CC} = 3.0 V to 3.6 V [2]								
		C_L = 15 pF	-	4.2	12.8	1.0	15.0	1.0	16.5	ns
		C_L = 50 pF	-	6.0	16.3	1.0	18.5	1.0	20.5	ns
		V_{CC} = 4.5 V to 5.5 V [3]								
		C_L = 15 pF	-	3.2	8.6	1.0	10.0	1.0	11.0	ns
		C_L = 50 pF	-	4.6	10.6	1.0	12.0	1.0	13.5	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [4]	-	12	-	-	-	-	-	pF
74AHCT1G17										
t_{pd}	propagation delay	A to Y; V_{CC} = 4.5 V to 5.5 V [1][3]								
		C_L = 15 pF	-	4.1	7.0	1.0	8.0	1.0	9.0	ns
		C_L = 50 pF	-	5.9	8.5	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [4]	-	13	-	-	-	-	-	pF

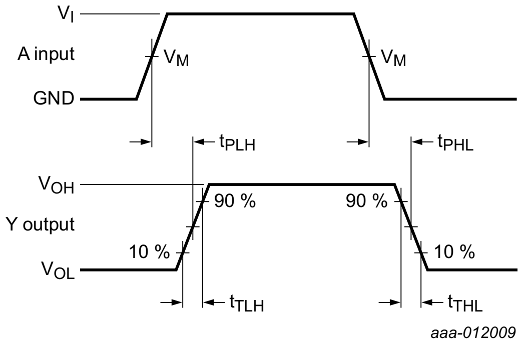
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] Typical values are measured at V_{CC} = 3.3 V.

[3] Typical values are measured at V_{CC} = 5.0 V.

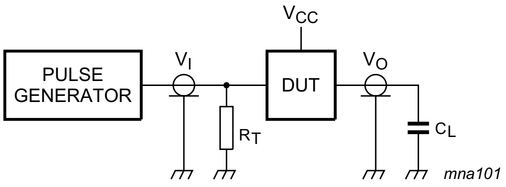
[4] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts.

13. Waveforms



The test data is given in Table 10

Fig 7. The input (A) to output (Y) propagation delays



Test data is given in Table 9.

Definitions for test circuit:

C_L = Load capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 8. Test circuit for measuring switching times

Table 10. Test data

Type number	Input		Output
	V_I	V_M	V_M
74AHC1G17	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT1G17	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$

13.1 Transfer characteristic waveforms

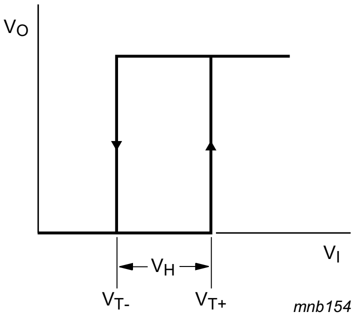


Fig 9. Transfer characteristic

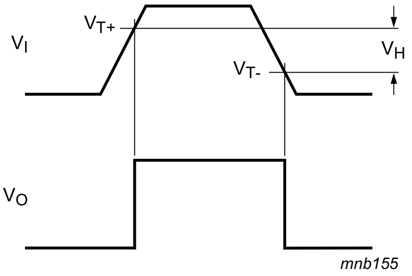


Fig 10. The definitions of V_{T+}, V_{T-} and V_H

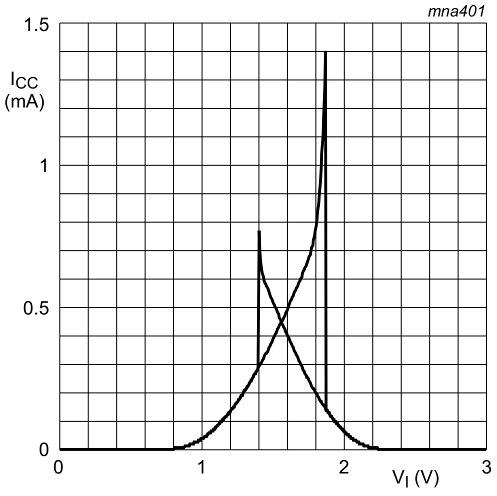


Fig 11. Typical 74AHC1G17 transfer characteristics; V_{CC} = 3.0 V

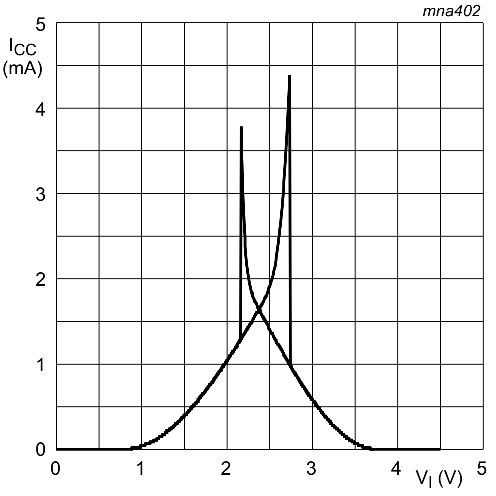


Fig 12. Typical 74AHC1G17 transfer characteristics; V_{CC} = 4.5 V

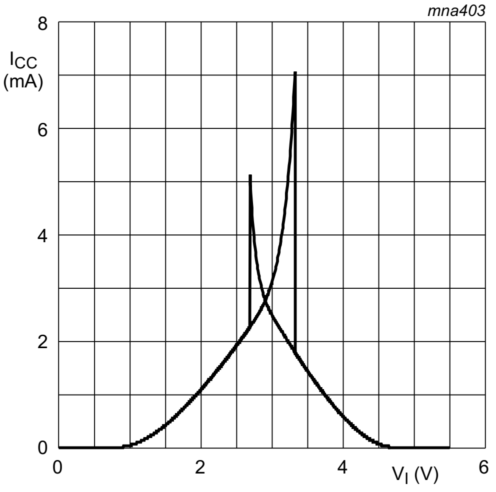


Fig 13. Typical 74AHC1G17 transfer characteristics; V_{CC} = 5.5 V

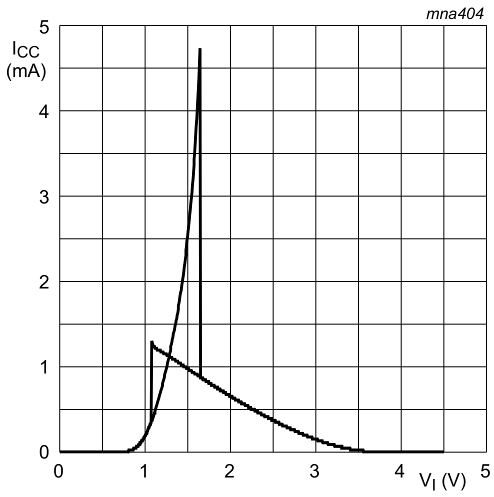


Fig 14. Typical 74AHCT1G17 transfer characteristics; V_{CC} = 4.5 V

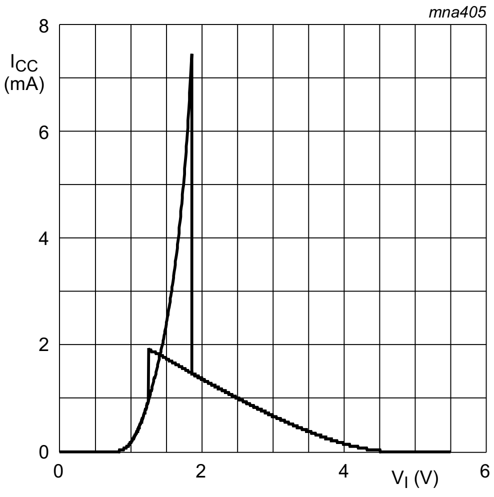


Fig 15. Typical 74AHCT1G17 transfer characteristics; V_{CC} = 5.5 V

14. Application information

The slow input rise and fall times cause additional power dissipation, which can be calculated using the following formula:

$P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC}$ where:

P_{add} = additional power dissipation (μW);

f_i = input frequency (MHz);

t_r = input rise time (ns); 10 % to 90 %;

t_f = input fall time (ns); 90 % to 10 %;

$\Delta I_{CC(AV)}$ = average additional supply current (μA).

Average additional I_{CC} differs with positive or negative input transitions, as shown in Figure 16 and Figure 17.

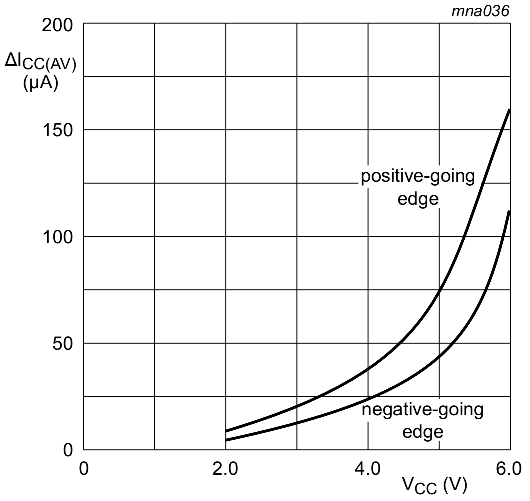


Fig 16. Average additional I_{CC} for 74AHC1G17 Schmitt trigger devices; linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$

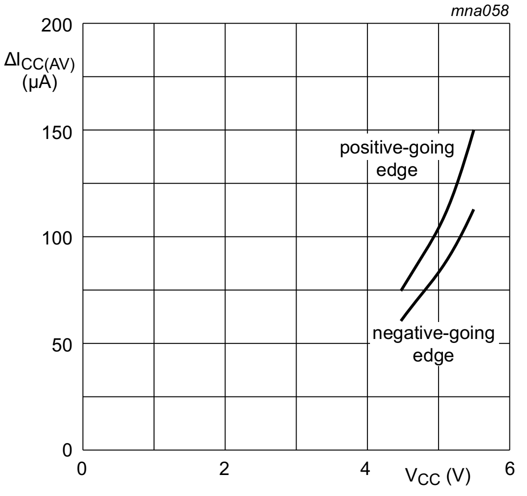
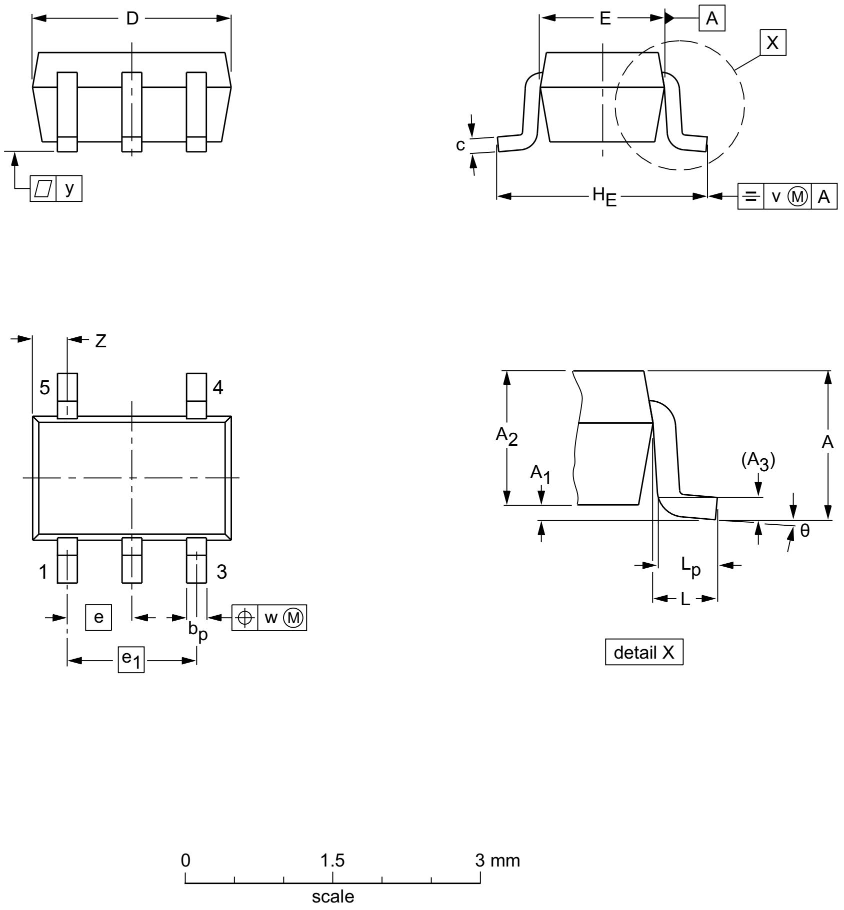


Fig 17. Average additional I_{CC} for 74AHCT1G17 Schmitt trigger devices; linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$

15. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

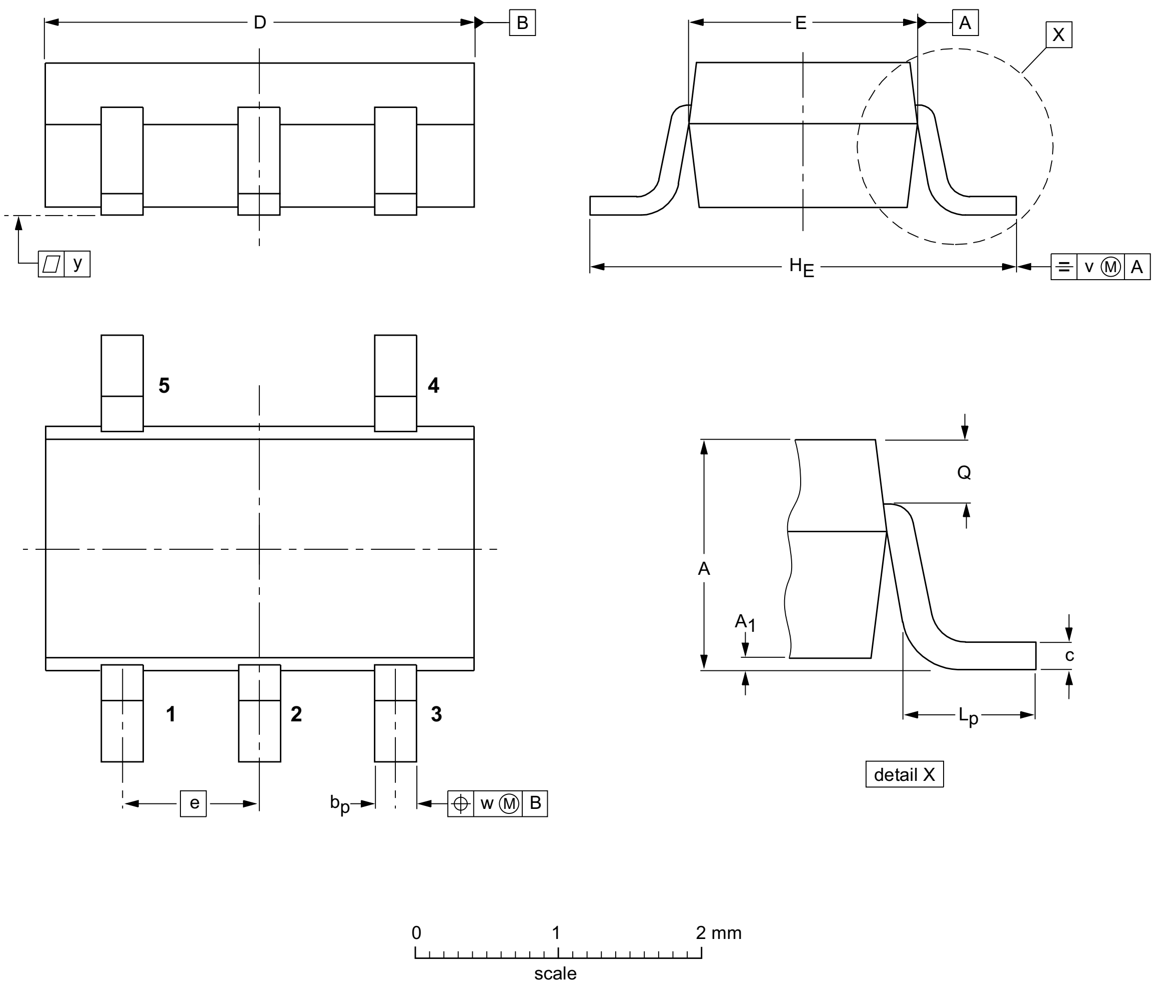
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~00-09-01~~ 03-02-19

Fig 18. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

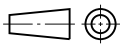
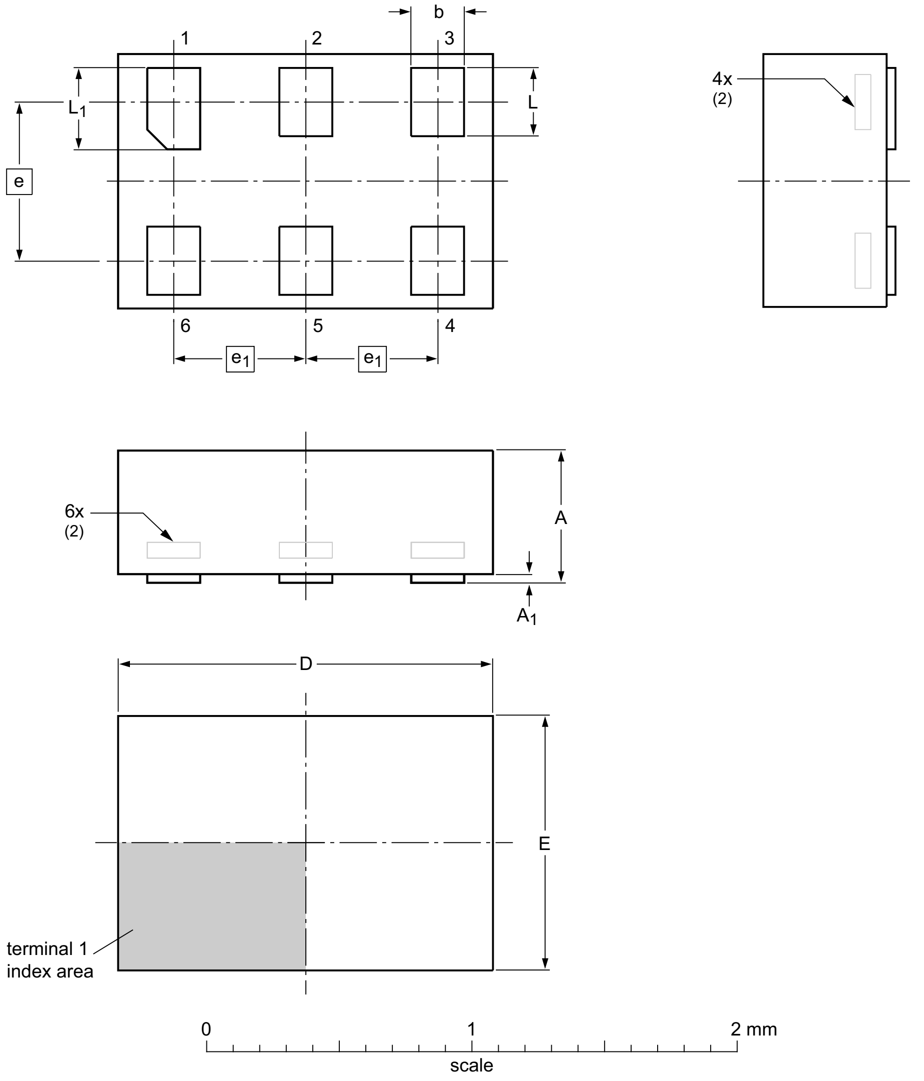
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig 19. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

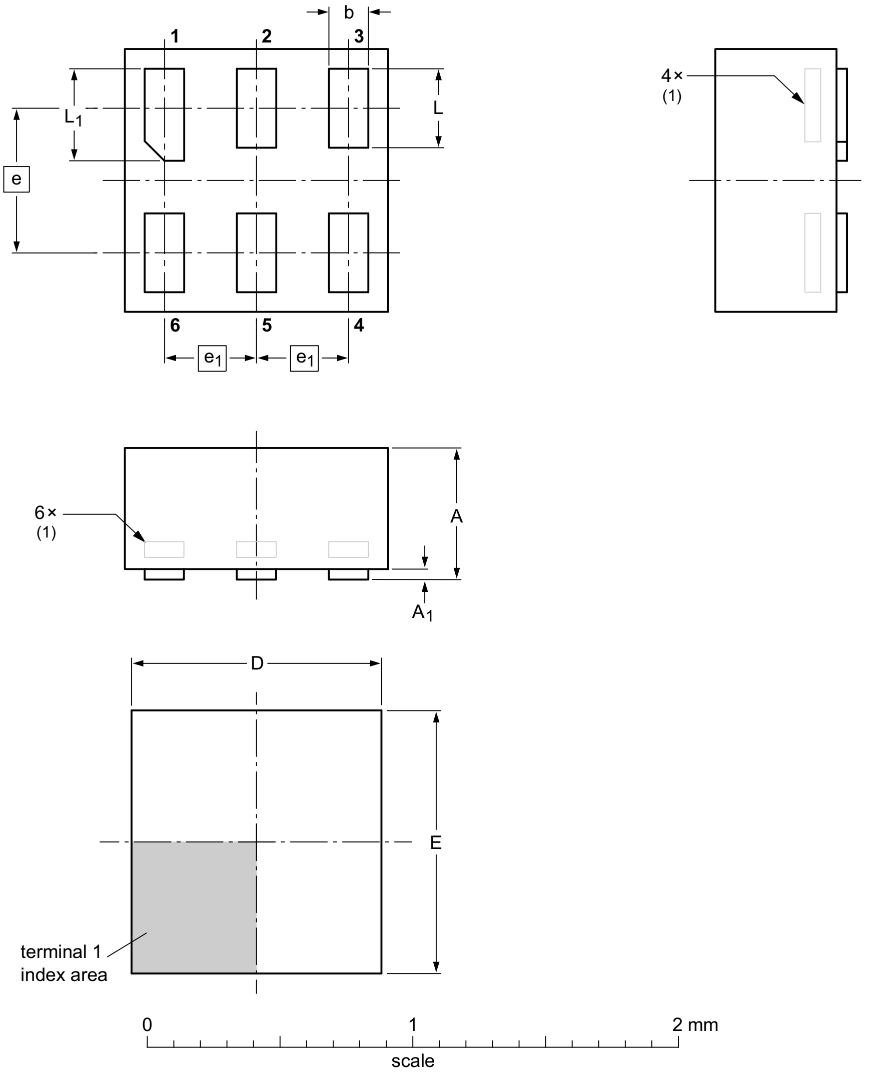
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig 20. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm **SOT891**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

Note

1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT891						~~05-04-06~~ 07-05-15

Fig 21. Package outline SOT891 (XSON6)

16. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

17. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G17 v.1	20140318	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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